Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Amended) A circuit for detection of internal microprocessor watchdog device execution comprising a microprocessor with the internal watchdog device, ~~and with~~ an input/output line transmitting information about microprocessor reset ~~, and~~ and a device for resetting the microprocessor system, ~~characterized in that,~~ wherein to the input/output line (11) transmitting information about the microprocessor (6) reset, a clock input CK is connected, which triggers the flip-flop (12), whose data input D and an inverted reset input /R are connected to ~~the~~ an output of the device (19) for resetting the microprocessor ~~system~~, and ~~the~~ an inverted flip-flop (12) output /Q is connected to ~~the~~ an input of the device (19) for resetting the microprocessor ~~system~~.

Claim 2 (Amended) The circuit according to claim 1, ~~characterized in that~~ further comprising an external resistor (10) connecting the input/output line (11) transmitting information about microprocessor (6) reset ~~is connected to the~~ to a power supply voltage (V_{CC}) ~~through an external resistor (10)~~.

Claim 3 (Amended) The circuit according to claim 1, ~~characterized in that the~~ wherein reset of the microprocessor system resulting from the reset of the microprocessor (6) is performed when the inverted reset input /R and the flip-flop (12) data input D are in a high state and the clock input CK changes from a low to a high state.

Claim 4 (Amended) The circuit according to claim 1, ~~characterized in that the~~ wherein reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by a low state of the ~~flip-flop (12)~~ inverted reset input /R of the flip-flop (12).

Claim 5 (Amended) A method for reset of a microprocessor system ~~comprising~~ with a circuit for detection of internal microprocessor watchdog device

execution ~~, characterized in that, after disruption of microprocessor operation (6),~~ comprising the following steps:

setting an input/output line (11) of ~~the~~ a microprocessor ~~is set~~ to a high impedance state ~~and~~ after disruption of microprocessor operation;

sending a system reset signal, generated by a flip-flop (12), ~~is sent~~ to a device for resetting the microprocessor system ~~, and after finishing the resetting of the microprocessor system,~~; and

setting the input/output line (11) ~~is set~~ to a low state after finishing the resetting of the microprocessor system.

Claim 6 (Amended) The method according to claim 5, ~~characterized in that~~ wherein the microprocessor system is reset, when the flip-flop (12) has an inverted reset input /R, a data input D and a clock input CK, and the inverted reset input /R and the data input D are in a high state and the clock input CK changes from a low to a high state.

Claim 7 (Amended) The method according to claim 5, ~~characterized in that~~ wherein the reset of the microprocessor system resulting from the reset of the microprocessor (6) is blocked by imposing a low state on the flip-flop (12) inverted reset input /R.

Claim 8 (New) A circuit for detection of internal processor watchdog device execution comprising:

a microprocessor having an input/output;

an internal watchdog device linked to the microprocessor via reset signal lines and activating the microprocessor;

a flip-flop having a data input D, an inverted reset input /R connected with the data input D, an inverted output /Q for resetting the microprocessor and a clock input CK connected to the input/output of the microprocessor via an input/output line transmitting information about microprocessor reset;

a device for resetting the microprocessor and linked to the inverted output /Q and the inverted reset input /R of the flip-flop and the microprocessor; and

an external resistor connecting the input/output line transmitting information about the microprocessor reset to a power supply voltage.